BRAD J. BARTLEY

12903 E Exposition Dr
Aurora CO 80012
303.343.0914
bbartley@alum.mit.edu

OBJECTIVE: A position in the design of digital electronics, ASICs, or microprocessors.

WORK EXPERIENCE:

NVIDIA, September 2004 to June 2009 — Beaverton, OR

Logic Design Engineer

Designed the microarchitecture of a vector integer arithmetic and encryption unit, to be included in a next generation GPU. Starting with documentation of the fundamental operations, I:

- Wrote C code to simulate the operations.
- Divided the operations into logical groups, each of which could share a common datapath.
- Designed and documented the datapath of each subunit.

Platform Qualification Manager

- Hired and managed three evaluation and EMI engineers.
- Conceived and managed lab expansion including walk-in radiated emissions test chamber.
- Managed regulatory certification of next generation nForce motherboard.

Platform Qualification Engineer

- Completed testing and regulatory certification (FCC, CE, C-tick, BSMI, MIC) of nForce 680i motherboard.
- Performed functional and regulatory (e.g. EMI) qualification of new nForce chipset-based PC motherboard designs with PCI-Express, SLI, GbE, SATA, etc.

Sun Microsystems, October 2002 to August 2004 — Newark, CA

Wrote power-on diagnostic tests for Millennium (UltraSparc V) processor in Eagle system. Wrote in C and assembly making extensive use of SPARC ASIs. Participated in microprocessor module FMEA exercise.

SandCraft, Inc., May 1998 to August 2002 — Santa Clara, CA

SandCraft designed high performance MIPS64 ISA microprocessors for networking equipment.

System Bring-up Lead

- Specified and oversaw design and manufacture of an evaluation system for the SR71000, an 800MHz superscalar MIPS64 microprocessor. Debugged those boards in hardware lab.
- Used evaluation system to debug SR71000 and to implement a Random Code on Silicon environment, integrating a random code generator, an architecture level simulator, assembler, linker, and board level monitor software. Accumulated 30+ billion cycles of random code run on SR71000 processors.
- Debugged initial silicon of SR1-GX, a 400MHz superscalar MIPS64 microprocessor, in a system environment.

Verification Group

- Coded RTL design tool in Perl. Coded testbenches in Verilog.
- Implemented control logic for optimized nonrestoring integer divide (32 and 64 bit) in Verilog. Wrote C code to emulate the same algorithm so the instruction level simulator could match the RTL's divide-by-zero behavior.
- Wrote validation testcases in MIPS assembly.

Intel Corporation, July 1997 to May 1998 — Hillsboro, OR

Component Design Engineer. Wrote and maintained in Perl simulation run tools in support of Pentium 4 validation.

EDUCATION:

Massachusetts Institute of Technology

1997 Master of Engineering, Electrical Engineering and Computer Science.

Thesis: "The Service Processor Subsystem of the StarT-Voyager Network of Workstations". Designed and wrote boot code of the protocol processor subsystem (an embedded PowerPC 604) of StarT-Voyager (a cluster of workstations).

1996 Bachelor of Science, Electrical Science and Engineering.

EXPERIENCE, PROFICIENCIES, AND KEYWORDS

Perl, Python, C, C++, Verilog, Unix, Shell, CVS, Expect, MIPS, MIPS64, assembly
Lab experience, logic analyzer, VLSI testers, hardware debug, embedded software debug, PC architecture